EE429 - Project 6 - improved FET op-amp

Purpose:
The purpose of this project is design an improved operational amplifier using FETs, and sizing them like you would in designing an IC. You must use only one resistor.

What to do:

You need to design a three stage op-amp, to the following specifications:

DC Voltage gain = 75 dB minimum, unloaded. (see how much you can get)
Output impedance, design for 200 ohms.
Output voltage swing: 20 volts peak-to-peak, into 2K ohm load.
Power supply: + and - 15 volts.
Frequency response: DC to whatever. Do the best you can.
Use N-channel FETs with KP=20u, Lambda=0, Vto=1 (enhancement).
and P-channel FETs with KP=5u, Lambda=0, Vto=-1 (enhancement).
Try to minimize the area. Minimum feature size is 1u.
For all FETs, use lambda = .1 / L, where L is the channel length.

Procedure:

You need to determine any missing specs, and make sure that the specs are clear to you.

First, determine a reasonable topology, then determine component values.

For the first stage, use the design from project 4, but replace the resistors with current mirrors. Keep the amplifier transistors the same as they were, with a total current of 10 uA.

The second stage is a P-channel inverting common source stage, as before, but it should use a current mirror as the load. Choose a current of .1 ma, and design for a gain of 40 dB.

The third stage is a source follower, with a current mirror load. Choose a current of 10 mA.

Use a reference current of 10 uA for the N-channel current mirrors.

The design is expected to use 10 FETs. 7 will be N-channel. 3 will be P-channel.

After you are satisfied with the hand calculations, verify it with simulation. You must first verify the DC bias, then AC gain and frequency response, then the output voltage swing, using transient analysis.

Measure the open-loop frequency response magnitude and phase angle. Determine the uncompensated corner frequency and unity gain frequency.

In your Spice/Gnucap model, add the following capacitance parameters to both .model statements and measure it again.
cgdo=2e-10 cgso=2e-10 tox=50e-9

Determine the value of a compensation capacitor experimentally so the phase angle does not exceed 100 degrees for all frequencies for which the gain is larger than unity (0 db). This capacitor should be placed from drain to gate of the P-channel common source stage. After determining the compensation, again measure the corner frequency and unity gain frequency.

After all this, also measure the common-mode gain, and compare it to the differential-mode gain.

Measurements to hand in:

You need to prepare a data sheet for this op-amp, which should be presented just after the cover page of the report.

You need to measure (simulate) and present:

1. Differential mode gain, Bode plot with magnitude (dB) and phase.
2. Common mode gain, Bode plot with magnitude (dB) and phase.
3. Common mode (voltage follower) clip level.
4. Differential mode clip level.
5. Equivalent input offset voltage.
6. Power supply, current requirements at no signal.
7. Slew rate.
8. Harmonic distortion at 100 Hz, 1 kHz, 10 kHz, 40 dB closed loop gain, 1 volt p-p output into 10k load.

The cover sheet "Specifications" should include open loop gain, gain-bandwidth product, phase margin, and quiescent current.

What to hand in:

Your report should consist of the following sections:

1. A cover sheet, with a schematic on it.
2. Brief specifications, in two columns, requested and simulated, also on cover.
3. Detailed data sheet, 1-2 page summary, as a manufacturer would present.
4. Design calculations and verification.
5. Simulation procedures and results.
6. Discussion
7. References and acknowledgements

Discussion:

In your discussion, you should point out any difficulties with the procedure, including any deviations between the predicted results and the results obtained by simulation. You should also justify any design decisions you made. If you chose to relax any of the specs, justify it here.

References and acknowledgements:

List all sources of information here, including texts, faculty, and classmates. You will not be penalized for working together with other students, if you say so. You will be penalized if you claim the work of someone else as your own.

Due date:

This project is due [redacted]

8th Monday