EE420 Lab - Week 4

25th April 2005

1 Overview

For the next few weeks, we will be building the parts of an op-amp, then combining them to actually make an op-amp. Build it carefully because you will hopefully use it for the rest of the term.

Week 4 Differential pair. We build and test a differental amplifier. You get a bonus point for each resistor you can eliminate by using current mirrors.

Week 5 Adding a second voltage gain stage. One more transistor converts the diff-amp to an op-amp. We will use a PNP. You get a bonus for using a current mirror. This simple op-amp can't drive much of a load, but it should work.

Week 6 Class-B power stage. We will use some bigger transistors to build a power stage. Then we will add it to our op-amp. If all goes well, you should be able to get a few watts out of it.

Week 7 High frequency performance. We will experiment with frequency compensation of our op-amp. The goal is to try for the best slew rate and gain-bandwidth product that we can get.

Week_8 Active filter. We will build 3 variants of a one op-amp bandpass filter, and characterize them. There is a bonus if you use your op-amp, and it actually works.

Week_9 Comparitors and Schmitt triggers. We will use the op-amp as a comparitor, and build a Schmitt trigger circuit, and a square wave oscillator. There is a bonus if you use your op-amp, and it actually works.

Week_10 Sine wave oscillator. We will use the op-amp to build a Wein bridge or Phase shift sine wave oscillator. There is a bonus if you use your op-amp, and it actually works.

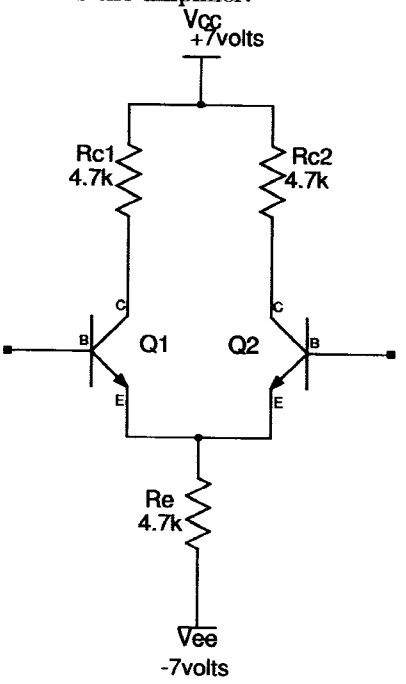
2 Objectives - week 4

1. To confirm the DC and AC characteristics of differential amplifiers.
2. To measure the differential input resistance, differential gain, and common-mode gain of a diff amp.
3. To compare the characteristics of a resistor biased amplifier to a current source biased amplifier.

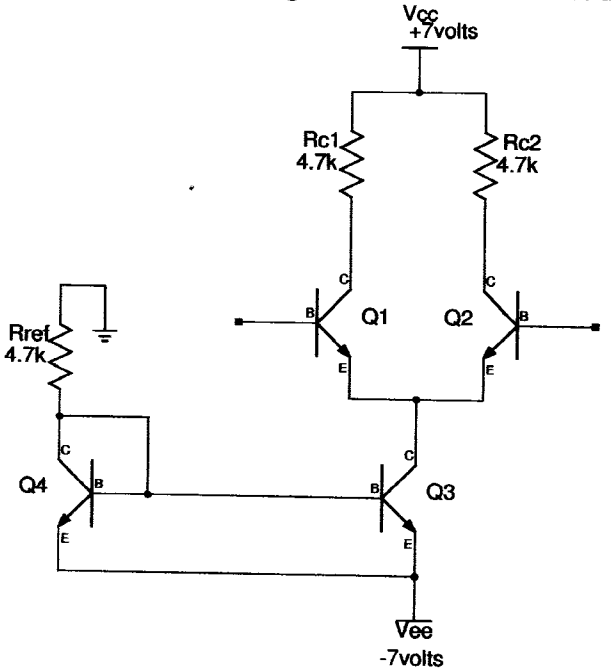
3 Background

In this experiment, we will explore the characteristics of a BJT differential pair (emitter coupled pair). This configuration is a major building block for multistage integrated circuit amplifiers. IC's use closely matched pairs, fabricated near each other on the same chip. We will use the LM3046 matched transistor array. The data sheet is attached.

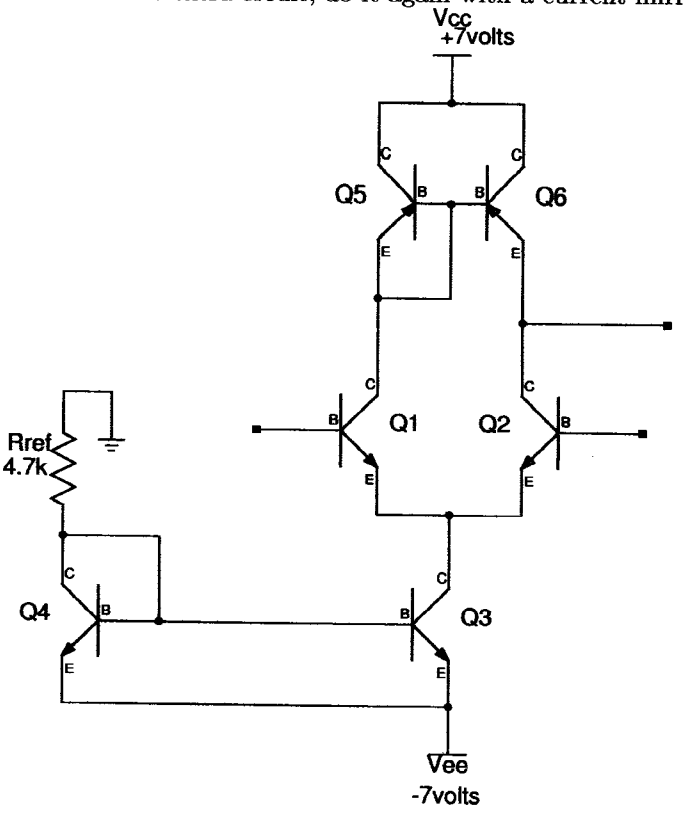
Here is the amplifier:



For extra credit, do it again with a current source in place of the emitter resistor:



For still more extra credit, do it again with a current mirror as the collector load:



4 Analysis (pre-lab)

4.1 Manual analysis

1. Perform a DC bias point analysis of the amplifier. Assume $\beta = \infty$, $V_{BE} = .7$ then set $V_{B1} = V_{B2} = 0$. Determine the values of all currents and voltages.

V_E	V_C	I_{EE}	I_C

2. Calculate the values of the small signal parameters at the calculated bias point.

g_m	r_π	r_e

3. Calculate:

   (a) The differential input resistance $r_{id} = v_{id}/i_b$

   (b) The single-ended differential gain $A_{d(se)} = v_{o2}/v_{id}$

   (c) The differential-output, differential gain $A_d = v_{od}/v_{id}$

   (d) The single-ended common-mode gain $A_{cm(se)} = v_{o2}/v_{icm}$

r_{id}	$A_{d(se)}$	A_d	$A_{cm(se)}$

4.2 Simulation

Using a simulator, verify the results you calculated. Check it for beta of 40, 100, and 200.

4.3 Current mirror bias (extra credit)

Replace $R_E$with the current mirror circuit, and repeat the analysis and simulation. Assume the Early voltage $V_A = 60$.

4.4 Current mirror load (more extra credit)

Replace R_{C1} and R_{C2} with a current mirror circuit, and repeat the analysis and simulation.

5 Experiment

1. Assemble the circuit as shown in the schematic. Use Q1 and Q2 for the diff-amp. Use the DVM to measure the 4.7k resistors. Choose $R_{C1}$and R_{C2} that are matched within 1% of each other. The actual value is not critical. The matching is critical. Make sure to connect the substrate (pin 13) to the negative supply rail. Lay it out as neatly as you can, using short leads. It should last through the term.

2. Connect both bases to ground and measure the quiescent voltages and currents. Verify that $V_{C1}$and V_{C2} are nearly equal. From the measured DC bias point, calculate the values for g_m.

V_E	V_{C1}	V_{C2}	I_{EE}	I_{C1}	I_{C2}

g_{m1}	g_{m2}	avg(g_m)

3. Use a voltage divider network in conjunction with your function generator to produce approximately 10 mV peak-to-peak triangular waveform at 1 kHz. Ground the base of Q_2 and apply the input signal to the base of Q_1.($v_{id} = v_{i1} - v_{i2} = v_{i1}$) Measure the value of v_{o2} and enter the values of $v_{id}$and $v_{o2(d)}$in the table. Calculate the gain. When using the oscilloscope, you may find it useful to use AC coupling, and set the bandwidth to 20 MHz. For best accuracy, you should set the scope so that the waveform nearly fills the screen.

v_{id}	$v_{o2(d)}$	$A_{d(se)}$

4. Insert a 2.7k resistor in series with each transistor base lead (a total of 5.4k differential source resistance) and note the decrease on output level. From this, calculate the input resistance.

v_{id}	$v_{o2(d.R_s)}$	R_{id}

5. Remove the voltage divider network and increase the amplitude of the function generator to approximately 2 volts peak to peak. Connect both bases together to the function generator. ($v_{i1} = v_{i2} = v_{icm}$) Measure the value of v_{o2} , calculate the gain, and enter the values in the table.

v_{icm}	$v_{o2(cm)}$	$A_{cm(se)}$

6. Compare your results to what you predicted.

5.1 Extra credit

1. Do it again with a current source in place of the emitter resistor.

2. For more extra credit, do it again with a current mirror in place of the collector resistors.

6 Report

6.1 Executive summary (on cover)

Show a schematic of the amplifier you measured, with its measurements in a table. If you did any extra credit options, show the schematic of the best amplifier, and the measurements for all of them.

6.2 More detailed summary

Write a paragraph on what you learned, and point out any surprises. Does it match the simulation? Explain. For the basic experiment, limit this section to one page. If you did any extra credit options, you may use two pages if you need it.

6.3 Journal

Provide a journal of what you did, with enough detail that someone else can reproduce your experiment and verify your work.

6.4 Simulation and analysis

If your results differ significantly from the simulation or analysis, try to find out why. Rerun the simulation if you need to.

7 Grading

For the basic experiment, the grade will be calculated according to the 10 point checklist.

If you did any extra credit options, extra points will be added as follows:

Up to 3 points (1 for the preliminary analysis, 1 for the experiment, 1 for the final report) will be added for the emitter current source.

Up to 6 points (2 for the preliminary analysis, 2 for the experiment, 2 for the final report) will be added for the current mirror load. This option requires significant extra work.

National Semiconductor

December 1994

LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

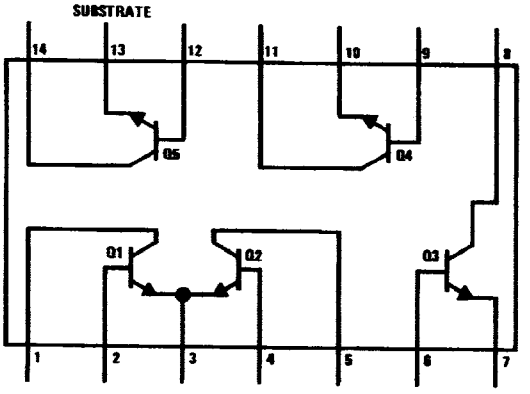
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) −55°C to +125°C

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line and Small Outline Packages



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Top View

Order Number LM3045J, LM3046M, LM3046N or LM3086N
See NS Package Number J14A, M14A or N14A

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (T_A = 25°C)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM3045		LM3046/LM3086		Units
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
T_A > 55°C			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
T_A > 75°C	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	−55°C to +125°C		−40°C to +85°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +85°C		
Soldering Information					
Dual-In-Line Package Soldering (10 Sec.)	260°C		260°C		
Small Outline Package					
Vapor Phase (60 Seconds)			215°C		
Infrared (15 Seconds)			220°C		

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Conditions	Limits LM3045, LM3046			Limits LM3086			Units
		Min	Typ	Max	Min	Typ	Max	
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10 μA, I_E = 0	20	60		20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10 μA, I_{CI} = 0	20	60		20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E 10 μA, I_C = 0	5	7		5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0.002	40		0.002	100	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			0.5			5	μA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V, I_C = 10 mA		100			100		
	V_{CE} = 3V, I_C = 1 mA	40	100		40	100		
	V_{CE} = 3V, I_C = 10 μA		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{O2} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.3	2				μA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1 mA		0.715			0.715		V
	V_{CE} = 3V, I_E = 10 mA		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4} \rvert$, $\lvert V_{BE4} - V_{BE5} \rvert$, $\lvert V_{BE5} - V_{BE3} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		−1.9			−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		0.23			0.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		1.1					μV/°C

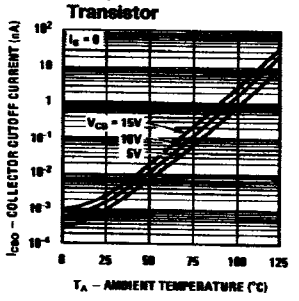
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

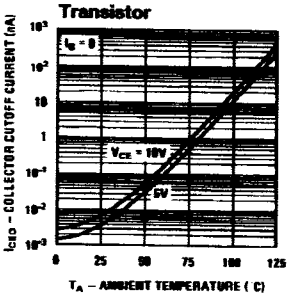
Parameter	Conditions	Min	Typ	Max	Units
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110 (LM3045, LM3046) (LM3086)		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3 + J 0.04		
Output Admittance (Y_{oe})			0.001 + j 0.03		
Reverse Transfer Admittance (Y_{re})			See Curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

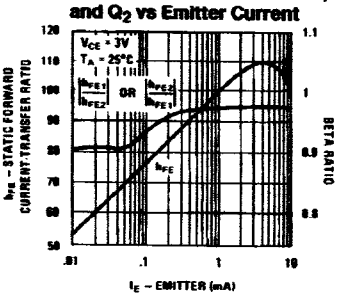
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor



Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current



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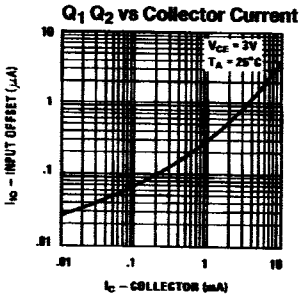
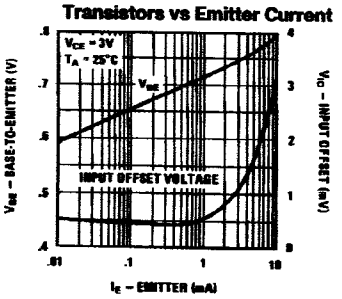
Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current



Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



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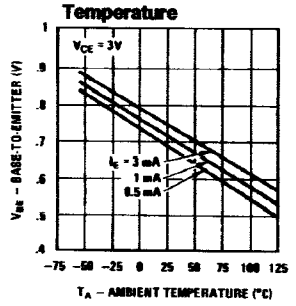
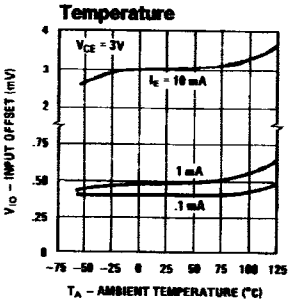
Typical Performance Characteristics (Continued)

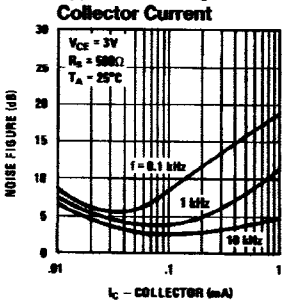
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

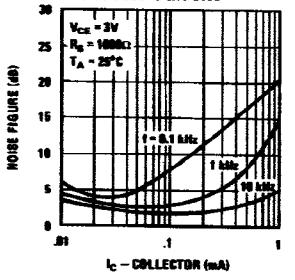


Typical Noise Figure vs Collector Current

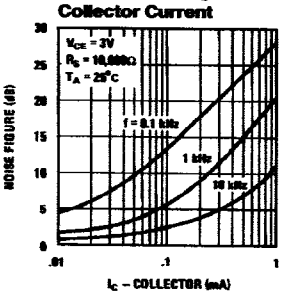


TL/H/7950–4

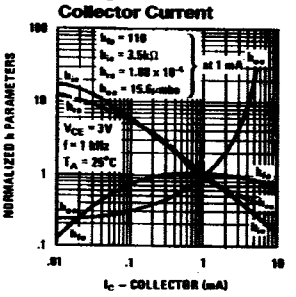
Typical Noise Figure vs Collector Current



Typical Noise Figure vs Collector Current



Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



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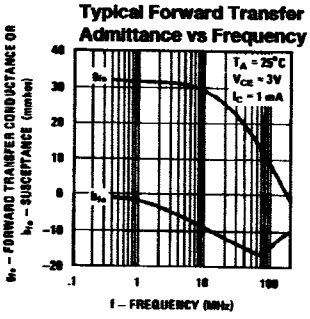
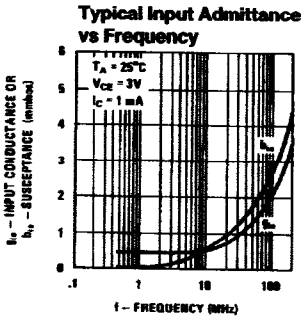
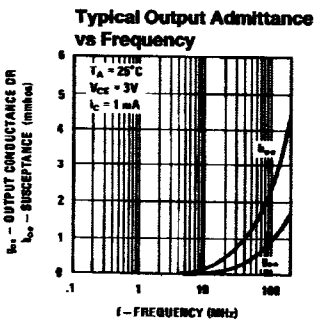
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency



Typical Output Admittance vs Frequency



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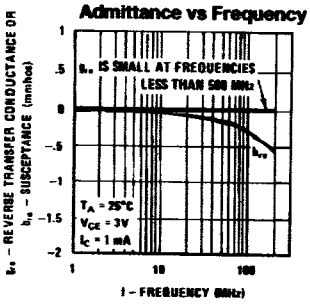
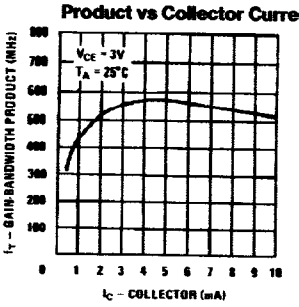
Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



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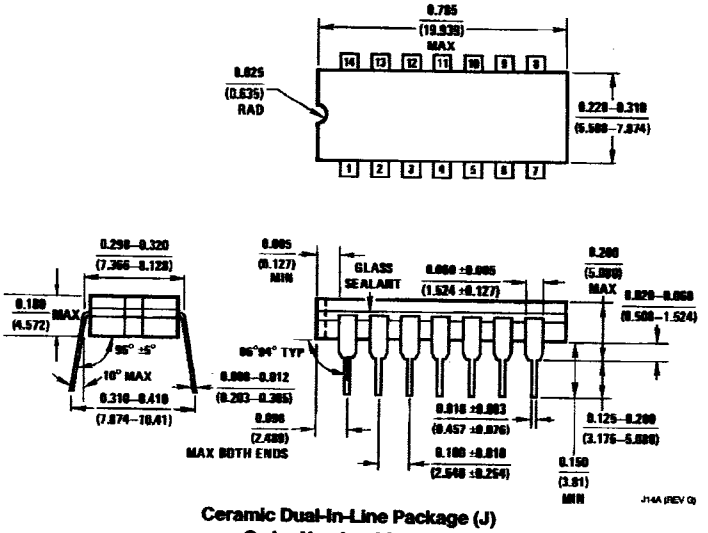
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number LM3045J
NS Package Number J14A