EE-420 Laboratory
A Discrete Multistage Amplifier

Objectives:

1. To confirm proper DC and AC operating conditions in a multistage amplifier.
2. To determine the overall AC characteristics of a multistage amplifier such as input resistance, voltage gain with load, voltage gain without load, output resistance, current gain, and power gain.
3. To determine individual stage voltage gains within a multistage amplifier.
4. To simulate a multistage amplifier.

Introduction:

Amplifiers are cascaded together in multistage configurations to achieve a variety of design goals. For instance a designer might wish to achieve high voltage gain, high input impedance, and low output impedance all within the same amplifier. By utilizing a multistage configuration, a designer can take advantage of the characteristics of the individual stages to achieve such goals, i.e. select an input stage that achieves high input resistance and an output stage that achieves low output resistance while an intermediate stage is responsible for high voltage gain. This is only one example of many possibilities.

An example of a discrete multistage amplifier that we will investigate in this laboratory is shown below in figure 1.

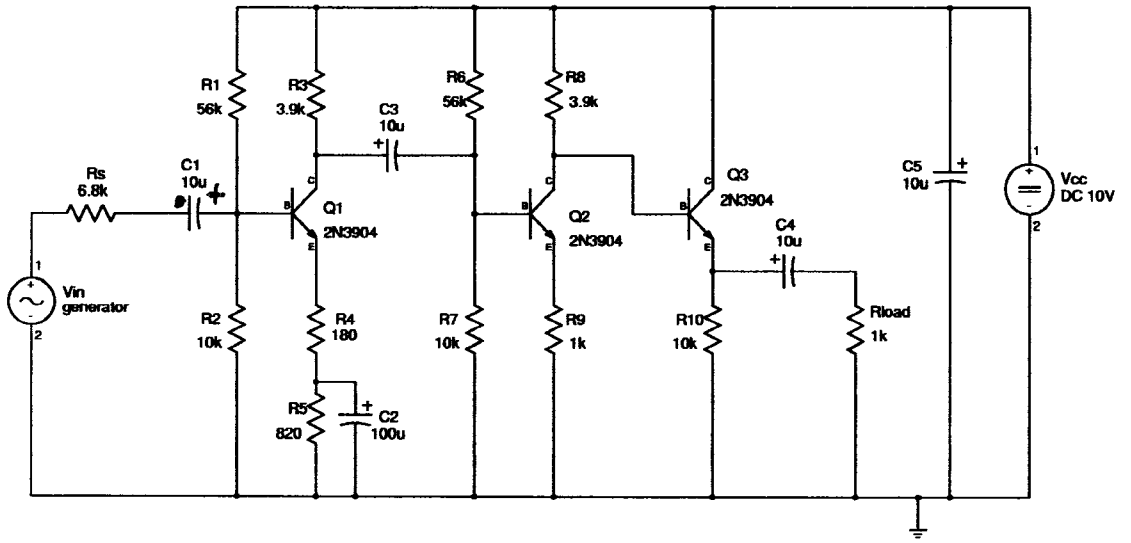

Figure 1

Week 1, DC Operating Conditions
in lab:

1. Build the first stage of the amplifier on your protoboard. Be sure to lay out the circuit neatly to assist in any necessary debugging. Make measurements of the node voltages, V_B, V_C, and V_E for Q_1 then calculate the values of I_C and V_{CE}. Enter these values in Table 1 when you are convinced the circuit is operating properly.
2. Continue by building and testing stage 2 and stage 3, sequentially. That is, build, test, and debug stage 2 before going on to stage 3. Complete Table 1. When interconnecting the stages with the coupling capacitors, note the polarity specifications of the electrolytic capacitors.
3. Compare the results to the simulation supplied by the professor.

Table 1. DC Bias Point Calculations

	I_C	V_{CE}
Q_1		
Q_2		
Q_3		

Table 2. DC Bias Point Measurements

	V_B	V_C	V_E	I_C	V_{CE}
Q_1					
Q_2					
Q_3					

Final report:

1. Perform a manual DC bias point analysis of each individual stage assuming the transistors have a $\beta = 100$. Record the values of the collector current, I_C, and the collector to emitter voltage, V_{CE}, that you expect for each transistor in Table 1, below.
2. Compare your calculations, the simulation, and your measured results.
3. Enter the circuit into a simulator. Run the simulator to find the voltages and currents. Compare this to what you expected.
4. Using the simulator, find all node voltages, VCE, VBE, IC, IB, IE, rpi, and gm for all transistors. Also find the DC current and power for the whole circuit.
5. Rerun the simulation for beta=200. Does it make much difference?
6. Rerun the simulation for beta=50. Does it make much difference?
7. Try to explain any significant differences between your results and expectations.

Week 2: AC Operating Conditions

Preliminary report:

1. Perform an ac small-signal analysis of the amplifier. First, calculate the small-signal parameters r_π, g_m, and $r_e = r_\pi/(1+\beta)$ using the calculated dc bias point information from Table 1 and enter the values in Table 3. Next, calculate the overall input resistance, R_i, output resistance, R_o, no load (NL) voltage gain, $A_{vNL} = v_{oNL}/v_i$, voltage gain with load, $A_{v(load)} = v_{o(load)}/v_i$, current gain, $A_i = i_o/i_i$, and power gain, $A_P = p_o/p_i$ and enter the results in Table 4.
2. Verify your results with simulation, using AC analysis at 1 kHz. Try it for beta = 100, 200, and 50.

In lab:

3. Set the function generator to produce a 1 kHz sinusoidal signal. Make sure the Rs = 6.8 kΩ source resistor and the R_L = 1 kΩ load resistor are connected.
4. Observe the output voltage signals of each stage of the amplifier with the oscilloscope and adjust the amplitude of the function generator so that there is no noticeable distortion of the signals. Make measurements required to complete Table 5.
5. Calculate the amplifier ac characteristics and fill in Table 6 using data from Table 5.

Table 3. Small-signal transistor parameters

	r_π	g_m	$r_e = r_\pi/(1+\beta)$
Q_1			
Q_2			
Q_3			

Table 4. Calculated amplifier ac characteristics

R_i	R_o	$A_{vNL} = v_{oNL}/v_i$	$A_{v(load)} = v_{o(load)}/v_i$	$A_i = i_o/i_i$	$A_p = p_o/p_i$

Table 5. AC Measurements

v_s	v_i	$v_{o(load)}$	v_{oNL}	$v_{o(stage\ 1)}$	$v_{o(stage\ 2)}$

Table 6. Amplifier ac characteristics

I_i	I_o

R_i	R_o	$A_{vNL} = v_{oNL}/v_i$	$A_{v(load)} = v_{o(load)}/v_i$	$A_i = i_o/i_i$	$A_p = p_o/p_i$

```
gnucap> log sim-commands
gnucap> get schemetic.ckt
* gnetlist -g spice-sdb schematic.sch
gnucap> list
************************************************************
* Spice file generated by gnetlist                         *
* spice-sdb version 10.9.2004 by SDB --                    *
* provides advanced spice netlisting capability.           *
* Documentation at http://www.brorson.com/gEDA/SPICE/      *
************************************************************
R5 ( 0 11 )  820.
Q3 ( 7 5 8 )  2N3904  area= 1.
R4 ( 11 3 )  180.
Q2 ( 5 4 6 )  2N3904  area= 1.
R3 ( 2 7 )  3.9K
Q1 ( 2 1 3 )  2N3904  area= 1.
R2 ( 0 1 )  10.K
C5 ( 7 0 )  10.u
Rload ( 0 10 )  1.K
R1 ( 1 7 )  56.K
Rs ( 12 9 )  6.8K
C4 ( 8 10 )  10.u
C3 ( 2 4 )  10.u
C2 ( 11 0 )  100.u
Vcc ( 7 0 )  DC  10.
R10 ( 0 8 )  10.K
R9 ( 0 6 )  1.K
C1 ( 9 1 )  10.u
Vin ( 12 0 ) GENERATOR
R8 ( 5 7 )  3.9K
R7 ( 0 4 )  10.K
R6 ( 4 7 )  56.K
.END
gnucap> print op v nodes
gnucap> build
>.model 2n3904 npn bf=100
>
gnucap> op
#
 300.15
gnucap> print op v(nodes)
op
#           v(1)       v(2)       v(3)       v(4)       v(5)       v(6)       v(7)       v(8)
    v(9)       v(10)      v(11)      v(12)
 300.15     1.457      7.3259     0.69253    1.457      7.3006     0.69253    10.        6.5377
    0.         0.         0.56787    0.
gnucap> print op vce(q*) vbe(q*) ic(q*) ib(q*) p(q*)
gnucap> op
#           vce(Q3)    vce(Q2)    vce(Q1)    vbe(Q3)    vbe(Q2)    vbe(Q1)    ic(Q3)     ic(Q2)
    ic(Q1)     ib(Q3)     ib(Q2)     ib(Q1)     p(Q3)      p(Q2)      p(Q1)
 300.15     3.4623     6.6081     6.6334     0.76296    0.76445    0.76445    647.3u     685.67u
    685.67u    6.473u     6.8567u    6.8567u    0.0022461  0.0045362  0.0045535
gnucap> print op vce(q*)
gnucap> op
#           vce(Q3)    vce(Q2)    vce(Q1)
 300.15     3.4623     6.6081     6.6334
gnucap> print op vbe(q*)
gnucap> op
#           vbe(Q3)    vbe(Q2)    vbe(Q1)
 300.15     0.76296    0.76445    0.76445
gnucap> print op ic(q*)
gnucap> op
#           ic(Q3)     ic(Q2)     ic(Q1)
 300.15     647.3u     685.67u    685.67u
gnucap> print op ib(q*)
gnucap> op
#           ib(Q3)     ib(Q2)     ib(Q1)
 300.15     6.473u     6.8567u    6.8567u
gnucap> print op ie(q*)
gnucap> op
#           ie(Q3)     ie(Q2)     ie(Q1)
 300.15    -653.77u   -692.53u   -692.53u
gnucap> print op rpi(q*)
gnucap> op
#           rpi(Q3)    rpi(Q2)    rpi(Q1)
 300.15     3.9957K    3.7721K    3.7721K
gnucap> print op gm(q*)
gnucap> op
#           gm(Q3)     gm(Q2)     gm(Q1)
 300.15     0.025027   0.02651    0.02651
gnucap> print ac v(vin) v(r2) v(r7) v(r10) v(rload)
gnucap> ac 1k
#Freq       v(Vin)     v(R2)      v(R7)      v(R10)     v(Rload)
 1.K        1.         0.47367    5.6216     19.269     19.267
gnucap> quit
```